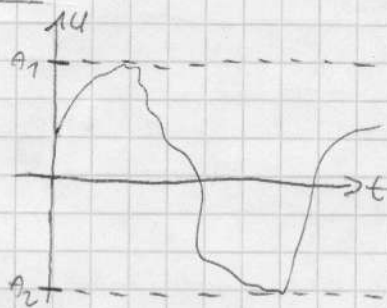
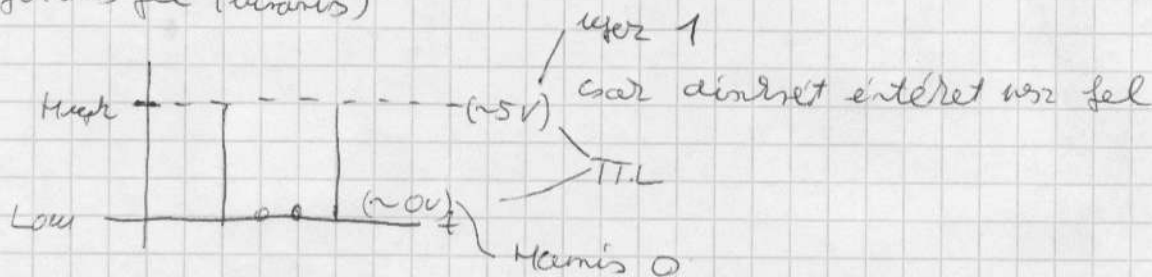


Analog fel:

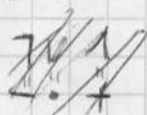


minden értéket felvehet

Digitális fel (kivétel)



Logikai áramkörök



NOT

Paritás: 1

Negáció: \bar{A}



Változóknak n értéket vehetnek fel

NOT		AND		OR			
A	Q	A	B	Q	A	B	Q
0	1	0	0	0	0	0	0
1	0	0	1	0	0	1	1
		1	0	0	1	0	1
		1	1	1	1	1	1

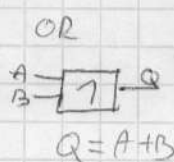
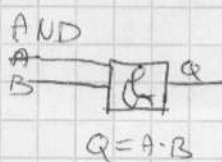
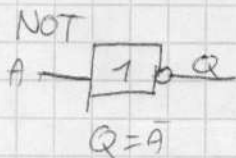
$Q = \bar{A}$
 $Q = A \cdot B$
 $Q = A + B$

referenciatablázat

$$Q = \bar{A}$$

$$Q = A \cdot B$$

$$Q = A + B$$



Logikai áramkörök:

- 1. kombinációs lánczat
- aritmetikai műveletek,
- szekvenciális áramkörök

6. Frege-Weierstrass (modern) Calculator

George BOOLE (1847)

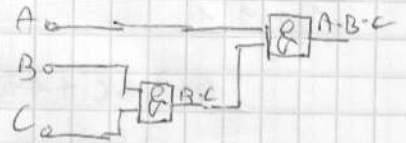
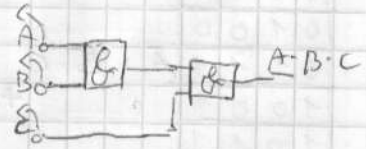
Assumptions:

1. Commutative

$$A \cdot B = B \cdot A$$

$$Q = A \cdot B \cdot C$$

$$A + B = B + A$$



2. Associative

$$A + B + C = (A + B) + C = A + (B + C) \dots$$

$$A \cdot B \cdot C = (A \cdot B) \cdot C = A \cdot (B \cdot C)$$

3. Distributive

$$a, A(B + C) = AB + AC$$

$$b, A + B \cdot C = (A + B) \cdot (A + C)$$

4. De Morgan

$$\overline{A \cdot B \cdot C} = \bar{A} + \bar{B} + \bar{C}$$

$$\overline{A + B + C} = \bar{A} \cdot \bar{B} \cdot \bar{C}$$

5. Absorption

$$A + A \cdot B = A$$

$$A \cdot (A + B) = A$$

6. Idempotence

$$A \cdot A = A$$

$$A + A = A$$

7. Complement

$$A + \bar{A} = 1$$

$$A \cdot \bar{A} = 0$$

$$A \cdot 1 = A$$

$$A + 0 = A$$

$$A + 1 = 1$$

Logikai függvény felírása

A	B	C	Q
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	1

Diszjunktív normál alak:

$$A \cdot B \cdot C$$

$$+ A \bar{B} \bar{C}$$

$$+ A \bar{B} C$$

$$+ A B \bar{C}$$

$$+ A B C$$

$$Q = A \cdot B \cdot C + A \cdot \bar{B} \cdot \bar{C} + A \cdot \bar{B} \cdot C + A \cdot B \cdot \bar{C} + A \cdot B \cdot C$$

$$Q = \bar{A} B C + A \bar{B} (\bar{C} + C) + A B (\bar{C} + C)$$

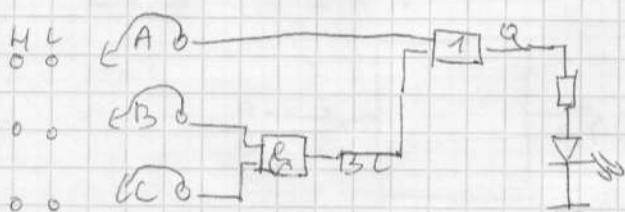
$$Q = \bar{A} B C + A \cdot \bar{B} + A B = \bar{A} B C + A(B + \bar{B})$$

$$Q = \bar{A} B C + A$$

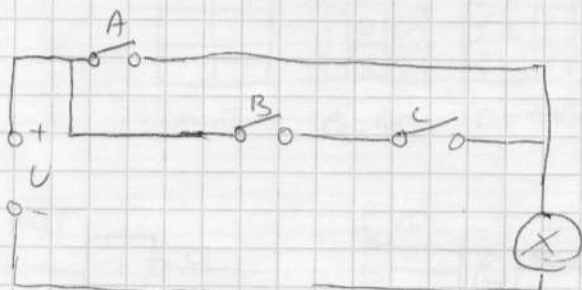
Shannon tétele: $A + B \cdot C = (A + B)(A + C)$

$$Q = (A + \bar{A})(A + B \cdot C) = \underline{\underline{A + B \cdot C}}$$

$$Q = A + B \cdot C$$



Kapcsolás logikai gép



Universellen Logikgatter

NAND

A	B	Q
0	0	1
0	1	1
1	0	1
1	1	0

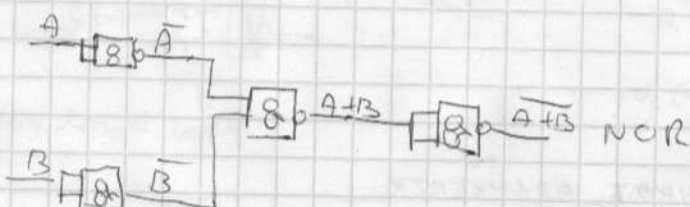
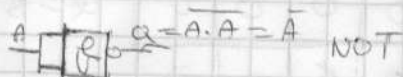
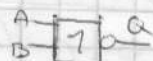
$$Q = \overline{A \cdot B}$$



NOR

A	B	Q
0	0	1
0	1	0
1	0	0
1	1	0

$$Q = \overline{A + B}$$



AND

Karnaugh-tabelle

A	B	Q
0	0	0
0	1	0
1	0	0
1	1	1

	0	1
A	0	0
1	0	1

n=2

	00	01	11	10
A	0	1	1	0
1	1	1	0	1

n=3

	0	1
00	1	1
01	0	0
11	1	1
10	1	1

n=3

Egyptenstil

	00	01	11	10
00	0	1	1	0
01	0	0	0	0
11	0	0	0	0
10	0	0	0	0

n=4

$$Q = \overline{A} \overline{B} D$$

$$Q =$$

$$Q = \overline{A} \overline{B} \overline{C} D + \overline{A} \overline{B} C D = \overline{A} \overline{B} D (\overline{C} + C) = \overline{A} \overline{B} D$$

	CD			
	00	01	11	10
AB	00	1	0	0
	01	1	0	0
	11	1	0	0
	10	1	0	0

	CD			
	00	01	11	10
AB	00	0	0	0
	01	1	1	1
	11	0	0	0
	10	0	0	0

$Q = \bar{C}\bar{D}$

$Q = \bar{A}B$

	CD			
	00	01	11	10
AB	00	0	0	0
	01	0	1	1
	11	0	1	1
	10	0	0	0

$Q = BD$

$Q = \bar{B}\bar{D}$

	CD			
	00	01	11	10
AB	00	0	0	1
	01	0	0	1
	11	0	0	1
	10	0	0	1

$Q = C$

LOGİKAT ARAHKÖRÖK

Q/TTL (transistor transistor logic)

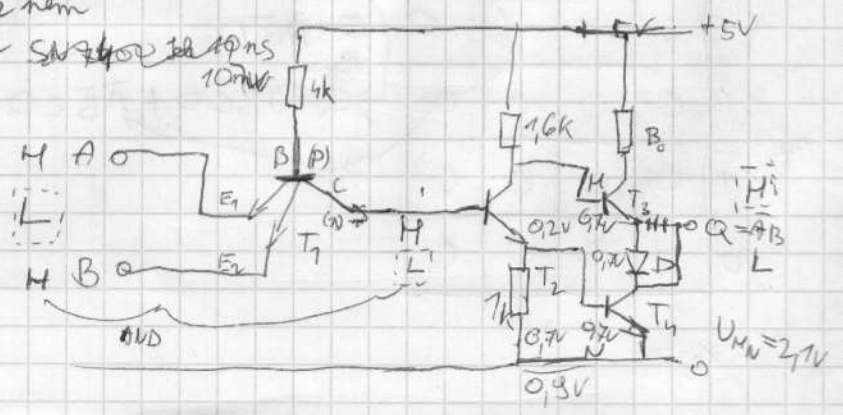
- TTL
 - Totem Pole (TP) (H, L)
 - Open collector (OC) (H, L)
 - Tri state (TS) (H, L, Z)

B/CMOS (Complementary Metal Oxide) (n saların + pozarın fet)

C/NMOS (Cox n saların fet)

TTL (TP) NAND

A	B	Q
0	0	1
0	1	1
1	0	1
1	1	0

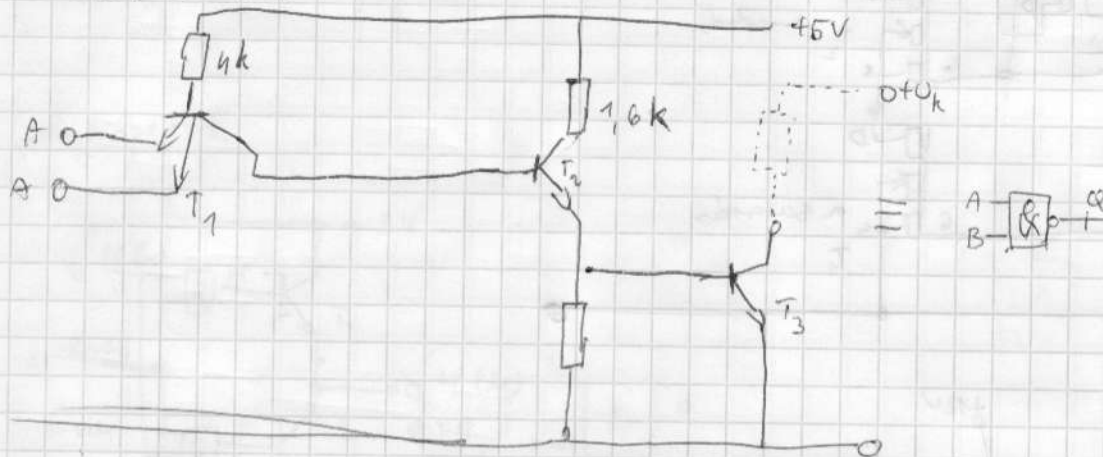


SN 7400 2el 10 ns
 10 mW
 SN 74500 3ns
 3mW
 LOW POWER SN 74000 3mW

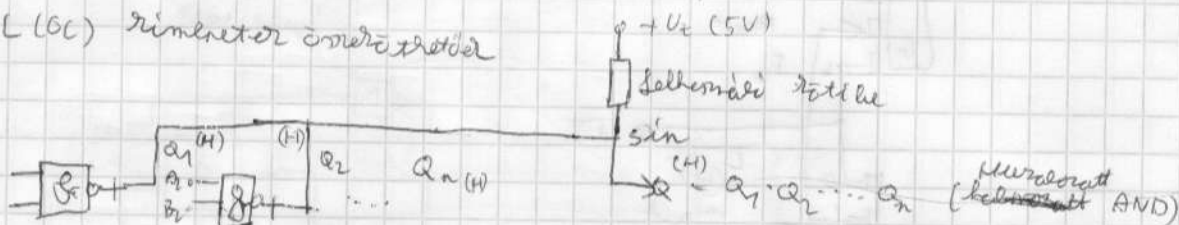
geringerer
 Leistungsverbrauch
 stattdessen



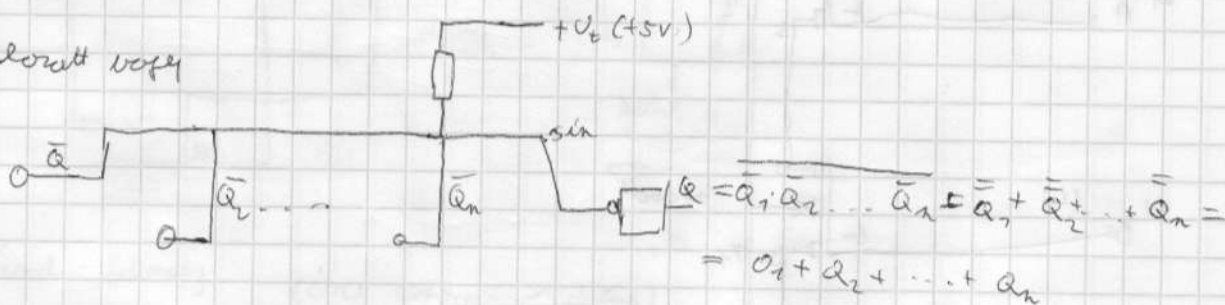
TTL (OC) NAND



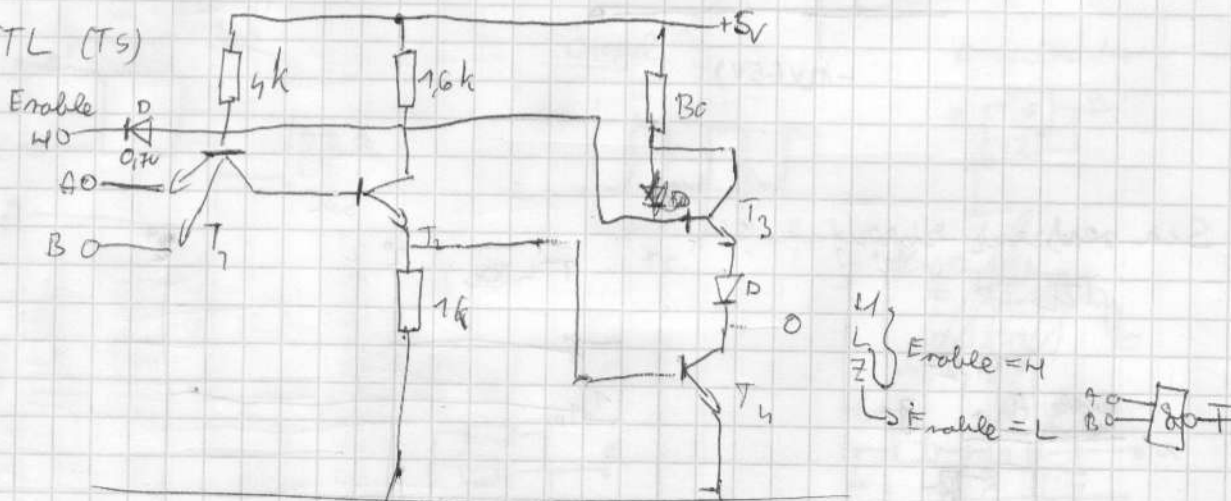
TTL (OC) Summen- oder Produktbildung



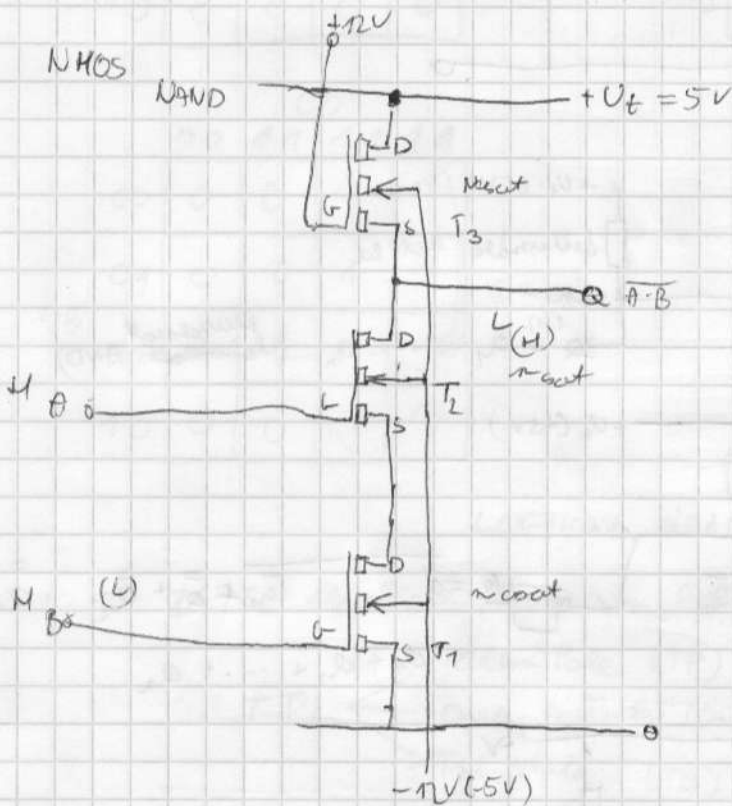
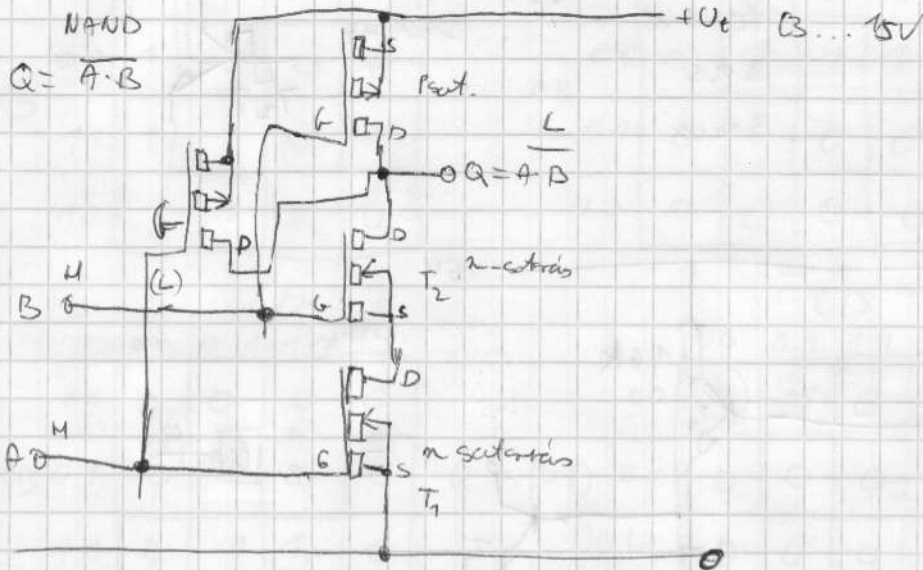
Mikrocontroller vorgef.



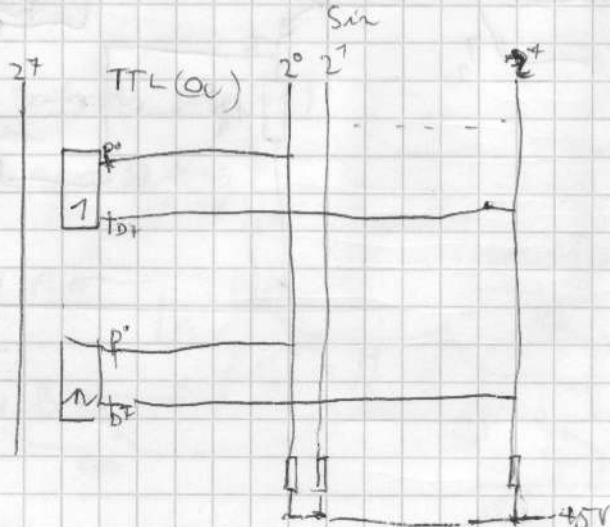
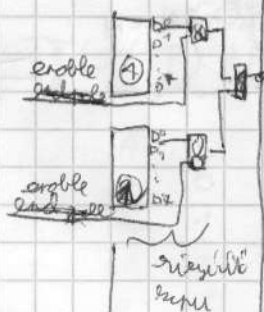
TTL (TS)



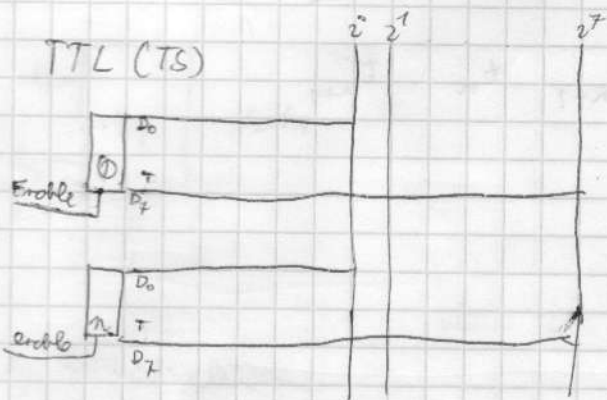
CMOS



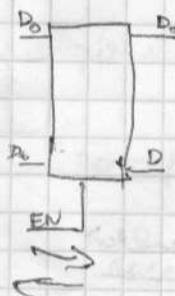
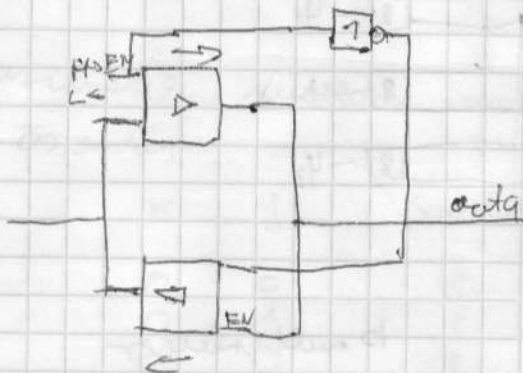
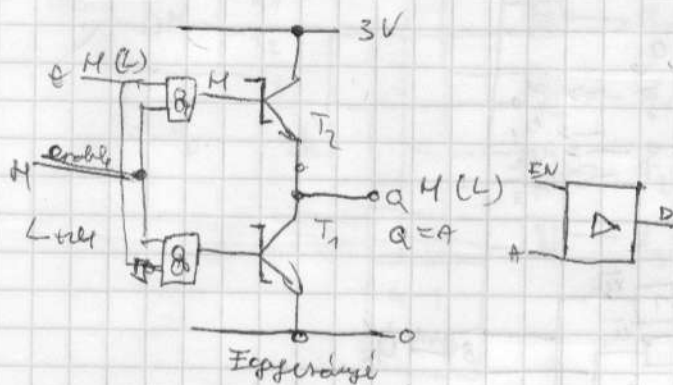
Sur redresseur: redressement sin



TTL (TS)



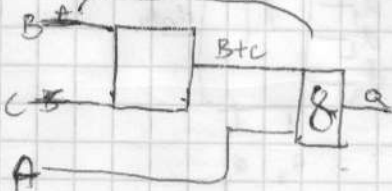
Sink-Schalter



Hazard - feldung

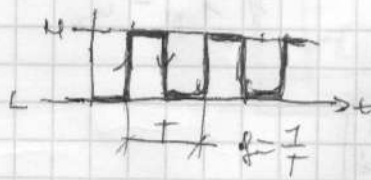
$$Q = A(B+C)$$

10ns

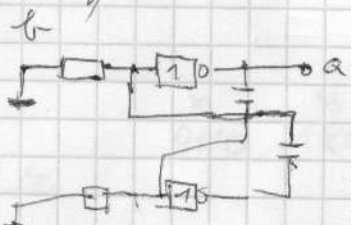
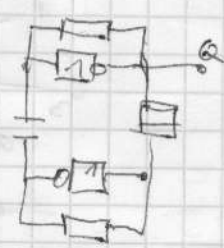
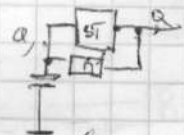


(one generator ellens)

Übergel



oscillator



Logikai ábrák: kombinációs ~~algoritmus~~ ^{algoritmus} ~~algoritmus~~

$t_{n-1} \quad t_n \quad t_{n+1}$

Kombinációs algoritmus:

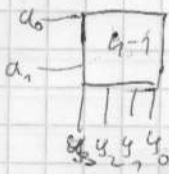
a , dekadák

$h-1$ dekadák

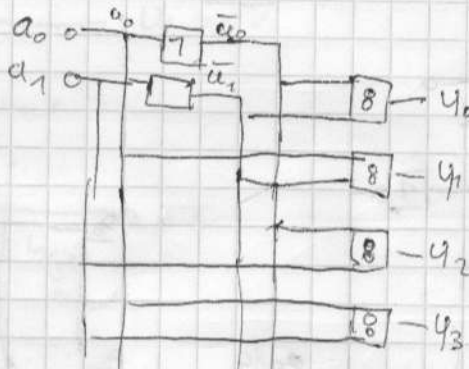
address: a

a_0, a_1 2 bits 2^2 értékek

a_0, a_1, a_2, a_3 4 bits $2^4 \dots$

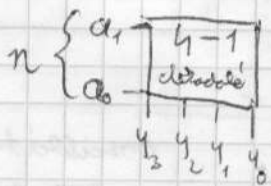


a_1	a_0	
0	0	$\rightarrow y_0$
0	1	$\rightarrow y_1$
1	0	$\rightarrow y_2$
1	1	$\rightarrow y_3$

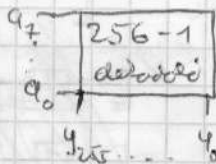


Kombinációs logika ~~algoritmus~~ ^{algoritmus}

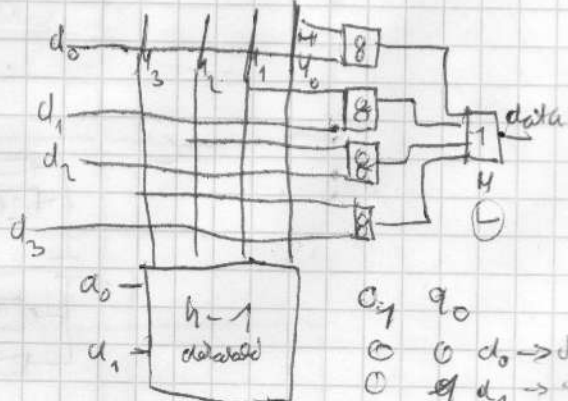
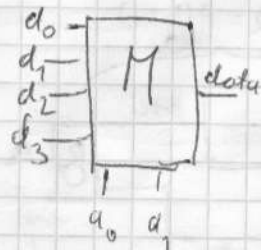
a



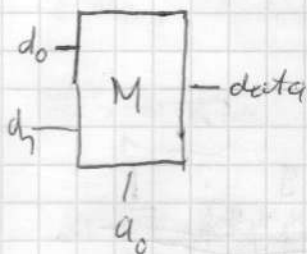
a_1	a_0	
0	0	$\rightarrow y_0$
0	1	$\rightarrow y_1$
1	0	$\rightarrow y_2$
1	1	$\rightarrow y_3$



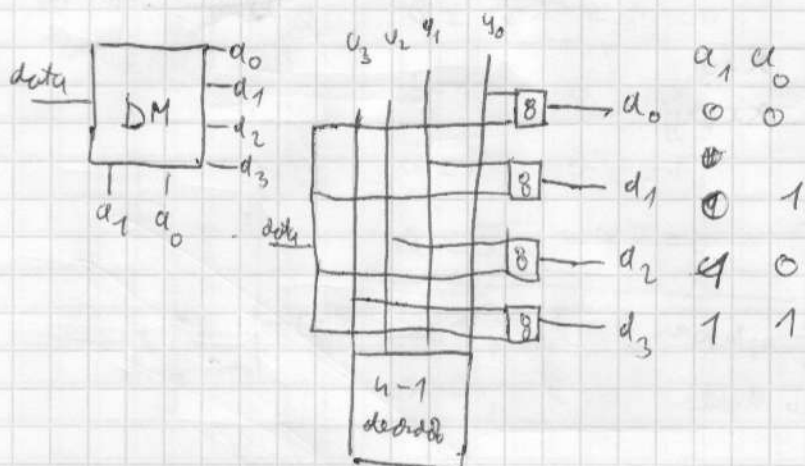
b multirétegű



a_1	a_0	
0	0	$d_0 \rightarrow y_0$
0	1	$d_1 \rightarrow y_1$
1	0	$d_2 \rightarrow y_2$
1	1	$d_3 \rightarrow y_3$



↳ demultiplexer



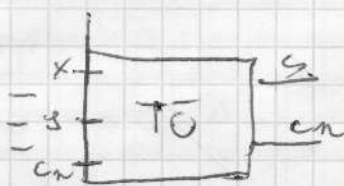
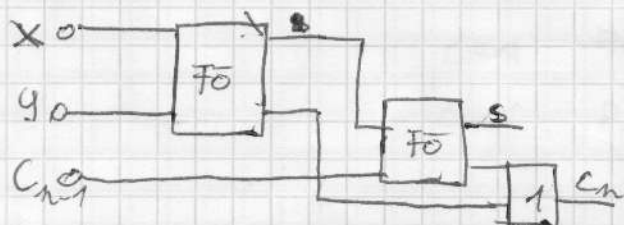
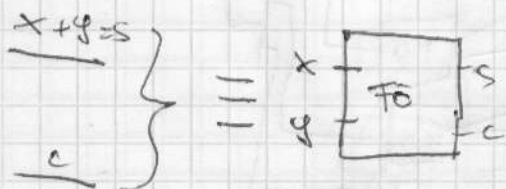
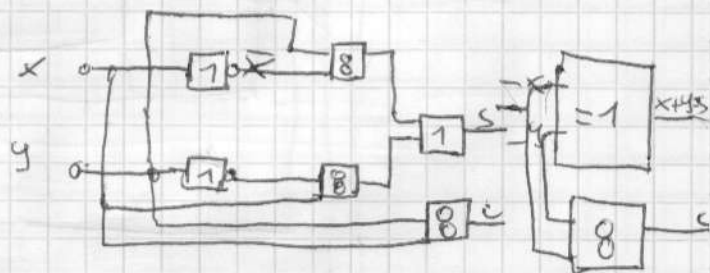
d aritmetikai művelet leírására logikai műveletre
 átváltás

x	y	Szám(s)
0	0	0
0	1	1
1	0	1
1	1	0

Logic(C)

$$\begin{aligned}
 &0 - \bar{x} \bar{y} \\
 &0 - \bar{x} y \\
 &0 - x \bar{y} \\
 &1 - x y
 \end{aligned}
 \left. \vphantom{\begin{aligned} &0 - \bar{x} \bar{y} \\ &0 - \bar{x} y \\ &0 - x \bar{y} \\ &1 - x y \end{aligned}} \right\} s = \bar{x}y + x\bar{y}$$

$$\underline{0 = x \cdot y}$$



x y
 0110 1100

Kérdés

$$x - y = 0$$

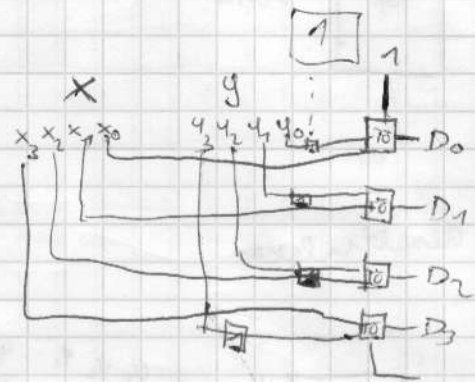
$$x + (-y) = 0$$

$$5 - 2 = 5 + (-2)$$

Kettős kiegészítés

$$\begin{array}{r} 0010 \\ + 1101 \\ \hline 1111 \end{array}$$

$$\begin{array}{r} 0101 \\ + 1110 \\ \hline 1001 \\ 00011 \end{array}$$



Háttérkérdés (+ -)

$$x + y$$

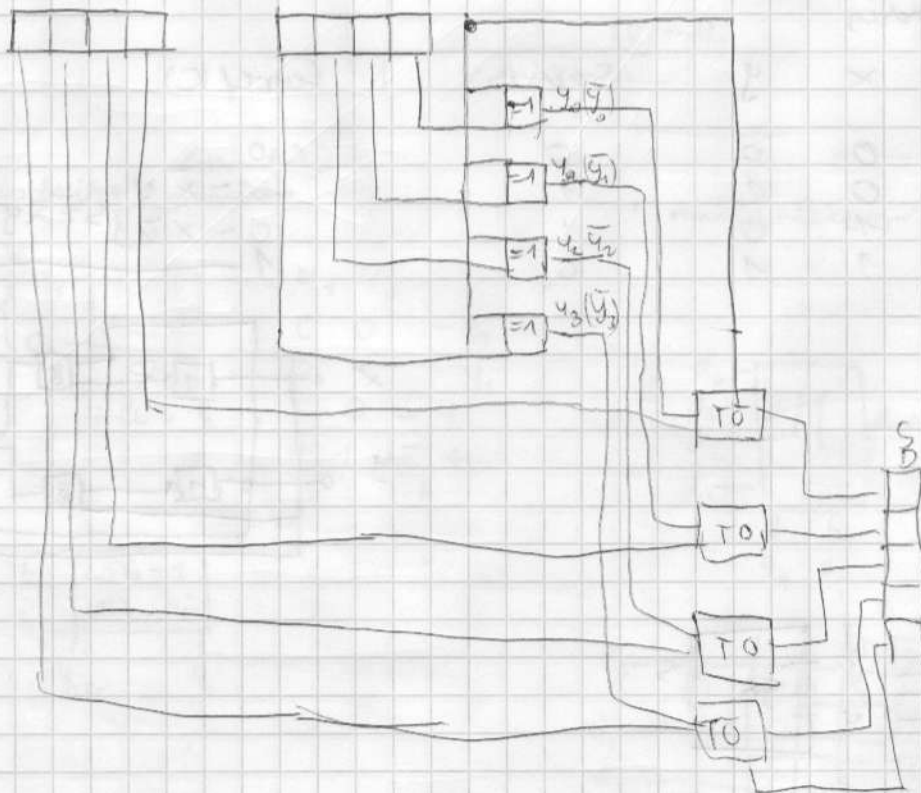
$$x + (-y)$$

Exor

a	b	a+b
0	0	0
0	1	1
1	0	1
1	1	0

művelet (+)
jel (-)

Négyesjegyű számok (S=0) és (S=1) ábrája



logikai kérdés / kalkulátor:

g/S - l társai ~~szabvány~~



$$S=0; R=1 \text{ leírás}$$

$$Q = S \cdot \bar{Q} = 0 \cdot \bar{Q} = 0 = 1$$

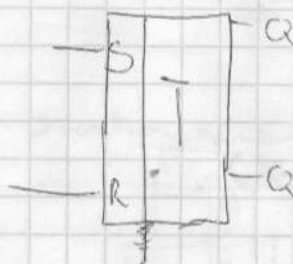


$$\bar{Q} = \bar{Q} \cdot 1 = 1 \cdot 1 = 0$$

$$S=1; R=0 \text{ törlés}$$

$$\bar{Q} = \bar{R} \cdot \bar{Q} = 0 \cdot \bar{Q} = 1$$

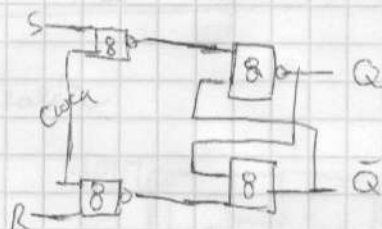
$$Q = S \cdot Q = 1 \cdot 1 = 0$$



$$S=1; R=1 \text{ megváltoztatás}$$

$$S=0; R=0 \text{ tiltott állapot}$$

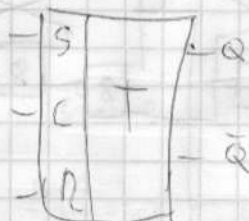
b/C - társai átviteli társai



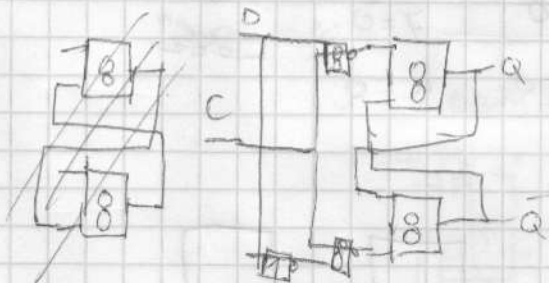
$$C=1 \begin{cases} S=1; R=0 \text{ leírás} \\ S=0; R=1 \text{ törlés} \end{cases}$$

$$S=0; R=0 \text{ elcsúsz}$$

$$S=1; R=1 \text{ tiltott}$$



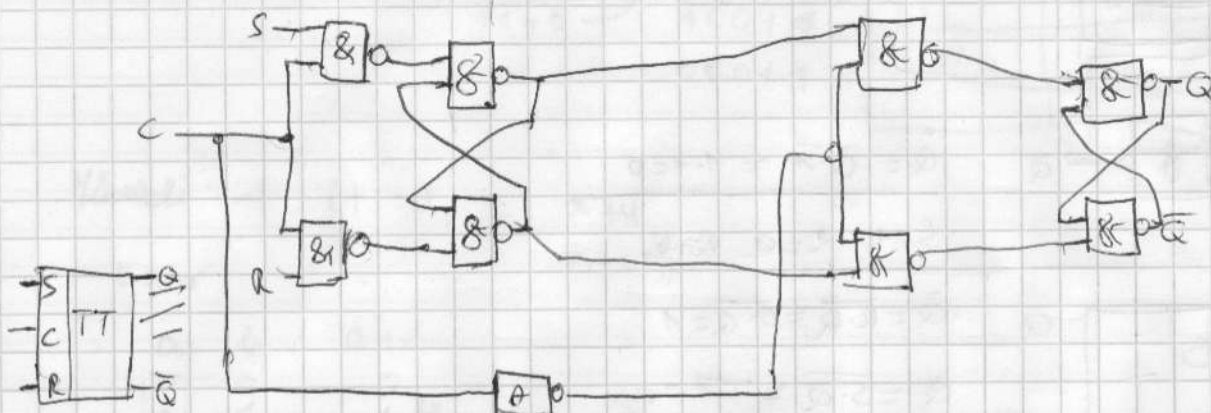
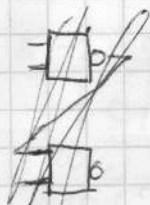
D - társai



$$C=1; D=1 \rightarrow Q=1$$

$$C=1; D=0 \rightarrow Q=0$$

Master Slave tároló



$C=1; S=1$ \uparrow \downarrow $\text{ébredés (M} \rightarrow \text{L)}$

$C=0; S=1$

$R=0$

$S=0$ $R=0$

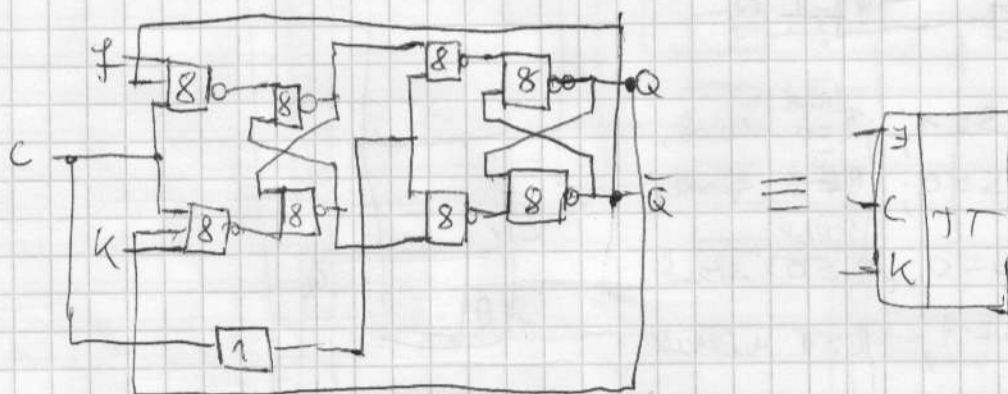
„szét” áll.

$S=1$ $R=1$

„feszít”

Törés $S=0; R=1$ $C=1$

J-K tároló



$C; J=1$ ind.; $K=0$

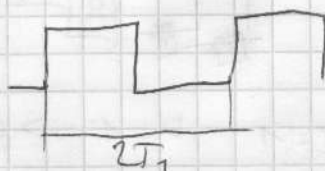
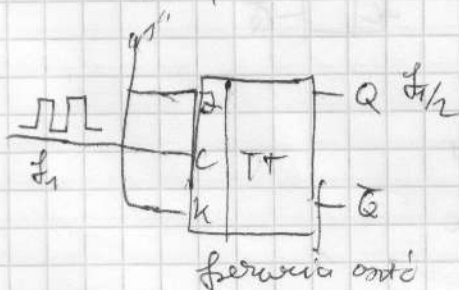
$J=0$

„szét”

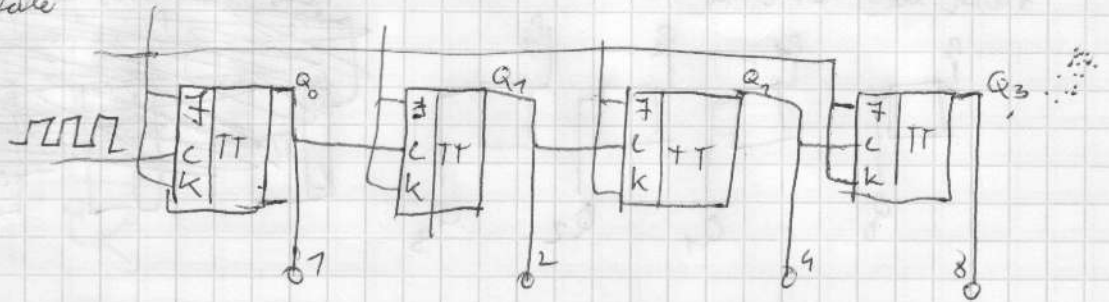
$K=1$ törés; $J=0$

$K=0$

$J=1$ $K=1$



Asunnen värkkö

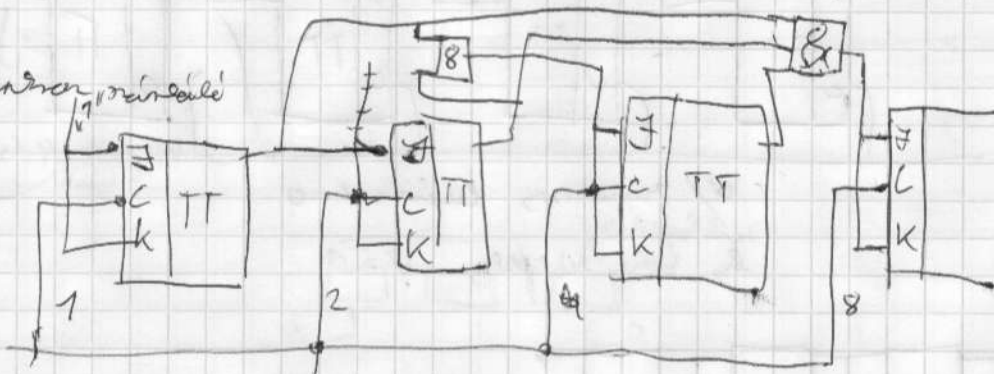


n	Q ₃	Q ₂	Q ₁	Q ₀
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	1	0	0	1
5	1	1	1	1

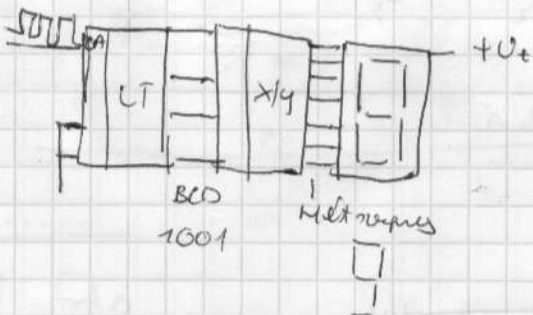
BCD



Suomen värkkö



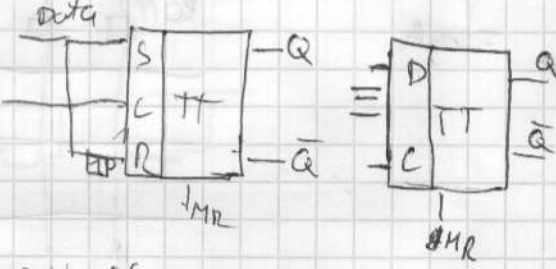
Dekoder



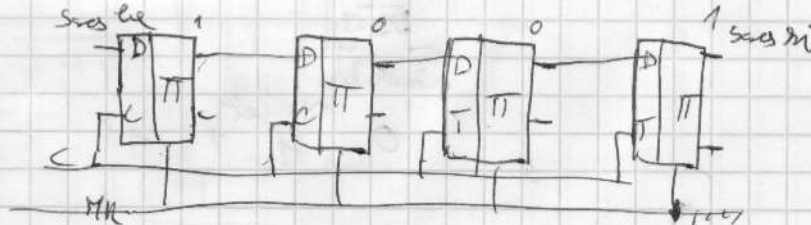
Suomen värkkö. Dekoder

Registrit

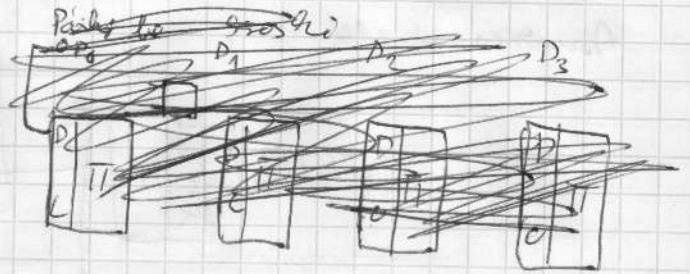
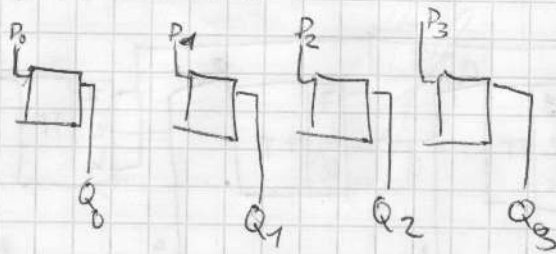
Q ₃	Q ₂	Q ₁	Q ₀
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1



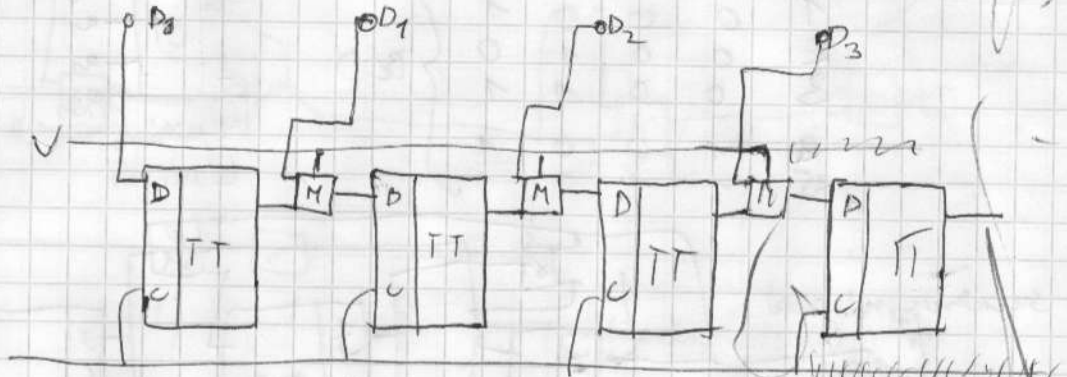
Registrit Dekoder



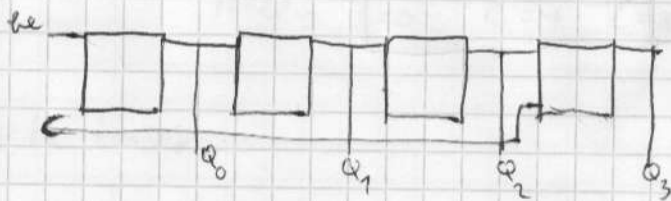
Pärh le länh 9i



Pärh a Series r



α / Tärhewas länh $V=0$
by Sars hilekka $V=1$



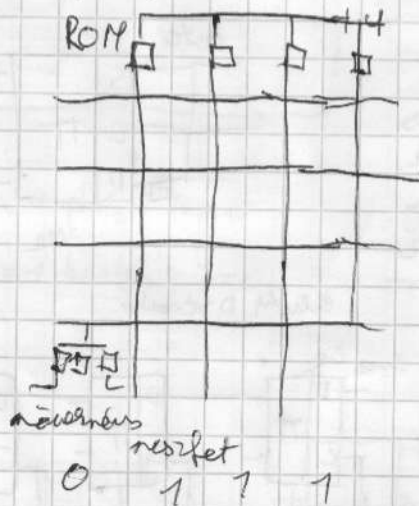
Read Only Memory (ROM)

PROM Programmable

EPROM Erasable

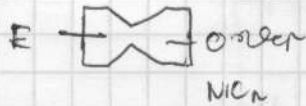
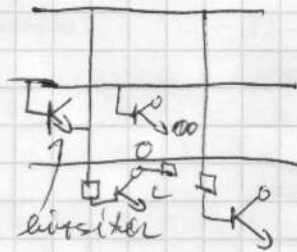
EEPROM Electrically

Flash

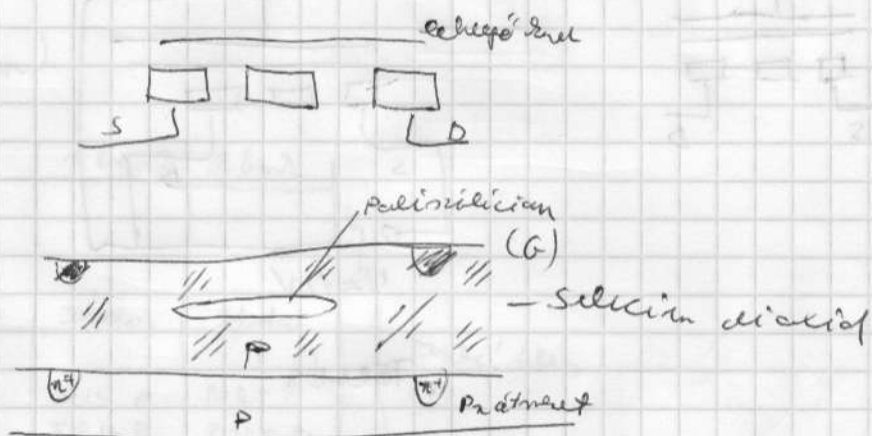


näwars
nawet
0 1 1 1

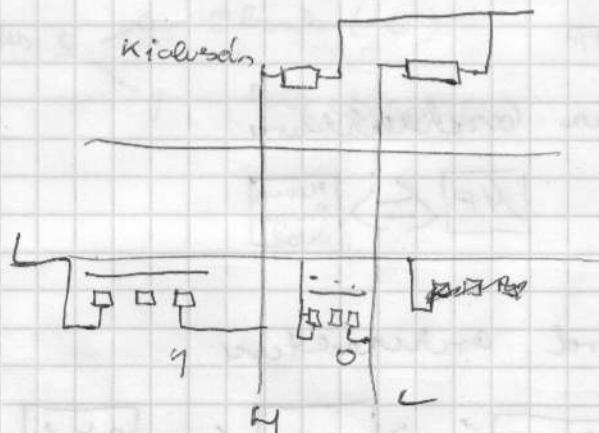
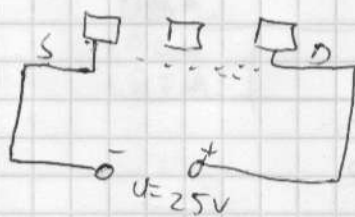
PRON



EPROM



Program



Törles

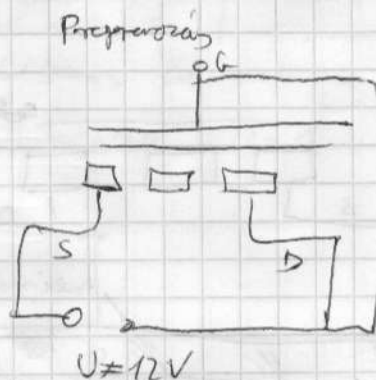
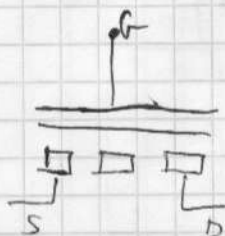
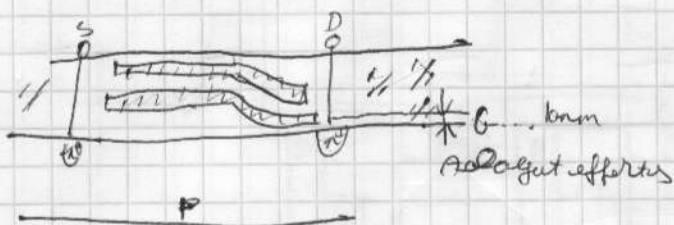


ultraviolet

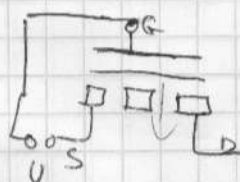
$$\lambda = 250 \text{ nm}$$

$$h\nu = 3,2 \text{ eV}$$

EEPROM
elektronisch
Programmable
Flash



Törles

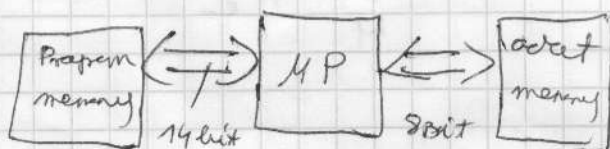


PIC 16784 μP

a, Neuman architecture



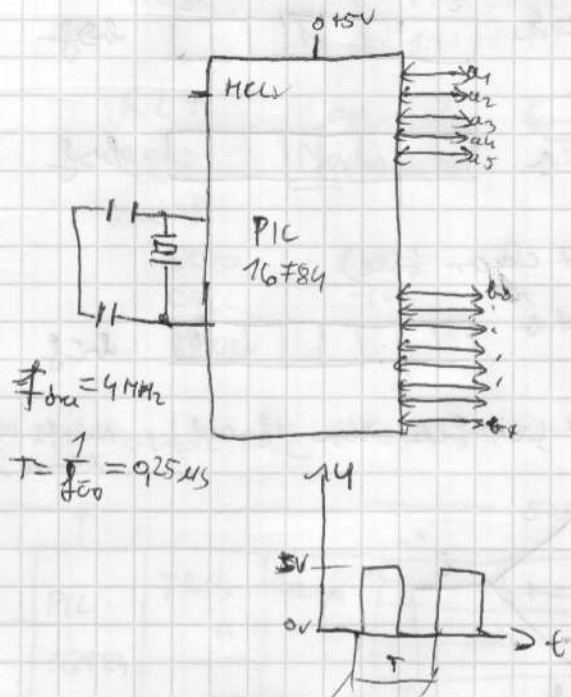
b, Harvard architecture



PLPIC 16784

RISC (reduced instruction set computer)

CISC (complex instruction set computer)



Adat memóriák (leírás)

Adatmemória	1. bank	0. bank
00h		
01h		
02h		
03h	status	status
04h		
05h	TRIS A	PORT A
06h	TRIS B	PORT B
07h		
08h		
09h		
0Ah		
0Bh		
0Ch		
0Dh		
0Eh		
0Fh		

Speciális

általános regiszter

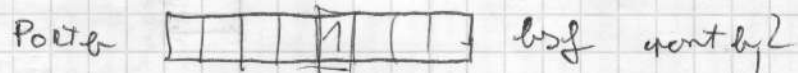
Statisztika 5

0 0 bank (C)

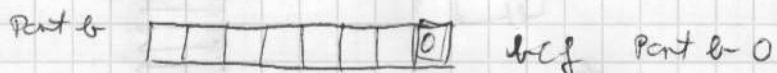
1 1 bank => Set (S)

Bitmanipulation instructions

BSF address, bit (bit set file)

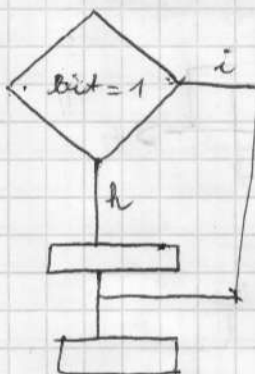


BCF address, bit (bit clear file)

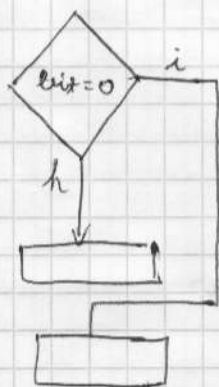


BTFS address, bit (bit test file skip if set)

Nexts are a relative address
upward



~~BTFS~~
BTFS



Byte manipulation instructions

CRF address

CRF#
work

INCF

DEC#

INCF#

DEC#

Address d
1 example
0 W.

Address d

Address d